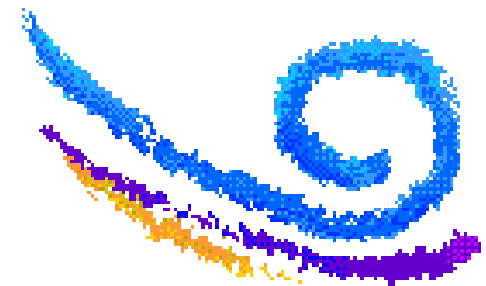


New Tricks for Old Dogs

Assembler Language - Big Picture

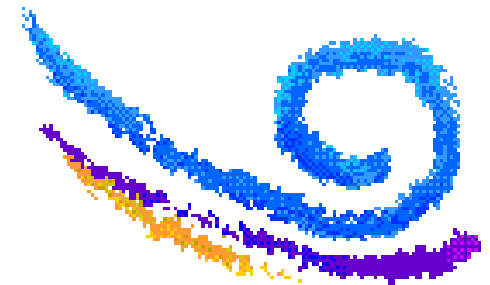
The Assembler - some changes

- ▶ Support for long data item names (up to 63 characters)
- ▶ Support for mixed case code
- ▶ Support for new data types
 - 64-bit integers
 - 64-bit addresses
 - Unicode character strings
 - IEEE floating point
- ▶ New Extended mnemonics (Jump)
- ▶ Labeled USINGs, dependent USINGs



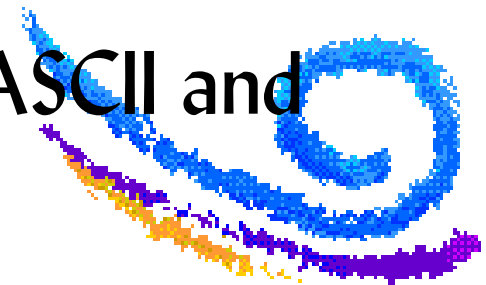
The Hardware - changes prior to z/Architecture

- ▶ Multiply Single (MSR, MS)
- ▶ Halfword Immediate (AHI, CHI, LHI, MHI, TMH, TML)
- ▶ Logical String Assist (CLST, CUSE, MVST, SRST)
- ▶ Extended long instructions (CLCLE, MVCLE, TRE)
- ▶ Relative Branching (BRAS, BRC, BRCT, BRXH, BRXLE)
- ▶ Unicode instructions (CUUTF, CUTFU)
- ▶ New floating point instructions (numerous)



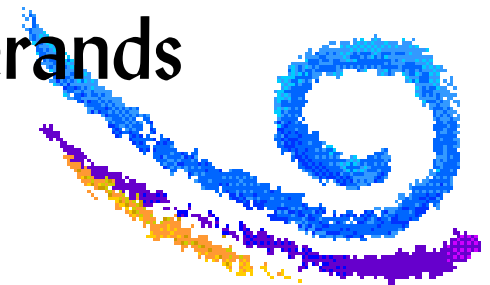
z/Architecture Instruction Additions

- ▶ Long branches - relative to current instruction
- ▶ Addressing mode switching and testing
- ▶ Specialized - EPSW
- ▶ Store and load instructions - all parts of 64-bit registers, from and to appropriate size memory locations
- ▶ ASCII support - pack and unpack
- ▶ Unicode support - pack and unpack
- ▶ Packed decimal instructions - TP plus the ASCII and Unicode pack and unpack



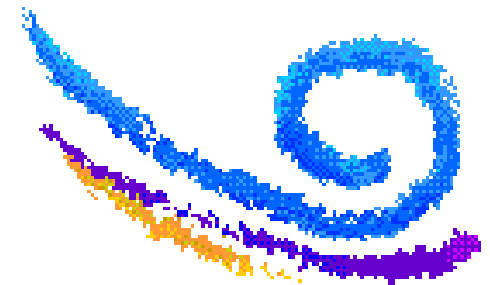
More z/Architecture Additions

- ▶ Binary arithmetic - combinations of 32-bit and 64-bit operands
- ▶ Logical binary - loading, storing, comparing, and logical arithmetic operations on 32-bit and 64-bit operands
- ▶ Bit-oriented instructions - ORs, ANDs and XORs of various size operands, new Test Under Mask variants
- ▶ Shift instructions - 64-bit operands
- ▶ Rotate instructions - 32-bit and 64-bit operands



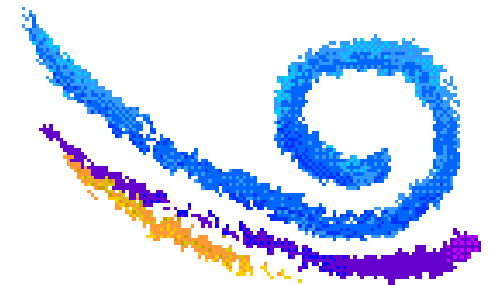
More z/Architecture Instructions

- ▶ Translate instructions - one or two byte inputs, one or two byte outputs
- ▶ Load / Store Reversed - to deal with endian issues
- ▶ Floating point <---> 64-bit integer conversions
- ▶ Classic_floating_point <---> IEEE_floating_point conversions



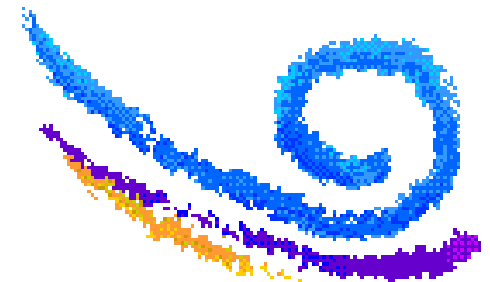
z/990 Instructions

- ▶ The advent of the z/990 machine introduced additional instructions (which are retrofitted to earlier z/Architecture machines)
 - Long displacement uses 20-bit displacements instead of the traditional 12 bits
 - Cryptographic instructions



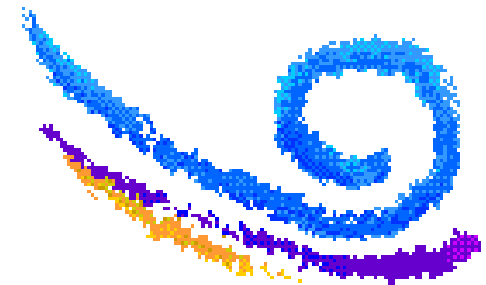
z9 Instructions

- ▶ The z9 series added a few instructions, such as
 - MVCOS - Move Characters with Optional Specifications
 - ECTG - Extract CPU Time
 - CSST - Compare and Swap and Store
 - Decimal Floating Point instructions



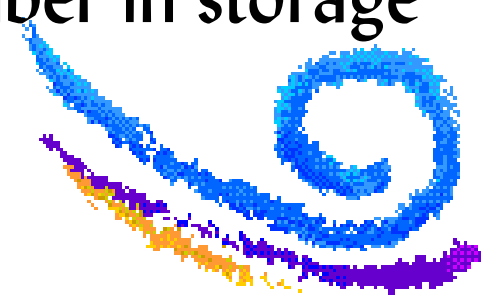
z10 Instructions

- ▶ The z10 series added many new instructions, such as
 - Data locations referenced using long displacements
 - Data locations referenced using relative displacements
 - Compare and branch in a single instruction
 - Compare and trap ("blow up")



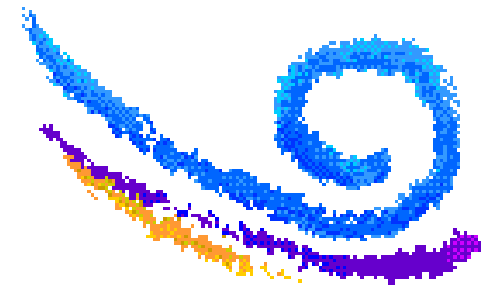
z10 Instructions, 2

- ▶ Additional z10 series new instructions
 - Additional compares with long relative displacements
 - Additional halfword immediate instructions
 - EXRL - EXecute Relative Long
 - Add immediate byte to 32-bit or 64-bit number in storage



z10 Instructions, 3

- ▶ Additional z10 series new instructions
 - New binary multiply instructions
 - Instructions to rotate bits in a register
 - Move immediate data to storage locations
 - New Translate and Test instructions





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